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Claims

[c1] A method of producing a fin structure, the method comprising:
providing a semiconductor substrate, an SiGe layer on said semiconductor substrate, and a silicon layer on said SiGe layer;
defining a fin portion of said silicon layer, said fin portion having thereunder a second portion of said SiGe layer;
forming a support structure attached to said fin portion and said semiconductor substrate; and
removing said second portion to form a first void between said fin portion and said semiconductor substrate.

[c2] The method of claim 1, wherein said support structure comprises portions of said SiGe layer not part of said second portion, and portions of said silicon layer not part of said fin portion.

[c3] The method of claim 1, wherein said support structure comprises a spacer material.

[c4] The method of claim 3, wherein said spacer material is selected from the group consisting of nitride, oxide,

oxynitride, and any combinations thereof.

[c5] The method of claim 1, wherein said support structure comprises a gate of a field effect transistor.

[c6] The method of claim 1, wherein said defining and forming steps are simultaneous.

[c7] The method of claim 6, wherein said support structure comprises portions of said SiGe layer not part of said second portion, and portions of said silicon layer not part of said fin portion.

[c8] The method of claim 7, wherein said defining and forming steps comprise:
depositing a first blocking layer on said silicon layer;
depositing a poly-silicon layer on said first blocking layer;
patterning said poly-silicon layer and said blocking layer to reveal a first portion of said silicon layer and a first portion of said SiGe layer, and producing a sidewall of said poly-silicon layer and a sidewall of said first blocking layer;
forming a first spacer on said sidewall of said poly-silicon layer and said sidewall of said first blocking layer to cover said fin portion and said second portion of said SiGe layer;

removing said first portion of said silicon layer to form a first sidewall of said silicon layer while said fin remains; and

removing said first portion of said SiGe layer to form a first sidewall of said SiGe layer while said second portion of said SiGe layer remains.

[c9] The method of claim 1, wherein said step of removing said second portion comprises selectively wet etching said second portion.

[c10] The method of claim 1 further comprising:
depositing an insulating material in said first void; and
removing said support structure.

[c11] The method of claim 10, wherein said insulating material is selected from the group consisting of an oxide, a nitride, oxynitride, low-k material, or any combinations thereof.

[c12] A fin structure produced by the method of claim 10, wherein said insulating material in said first void is asymmetrical.

[c13] The method of claim 7, wherein said defining and forming steps comprise:
depositing a first blocking layer on said silicon layer;
depositing a poly-silicon layer on said first blocking

layer;

patterning said poly-silicon layer and said blocking layer to reveal a first portion of said silicon layer and a first portion of said SiGe layer, and producing a sidewall of said poly-silicon layer and a sidewall of said first blocking layer;

forming a first spacer on said sidewall of said poly-silicon layer and said sidewall of said first blocking layer to cover said fin portion and said second portion;

removing said first portion of said silicon layer to form a first sidewall of said silicon layer while said fin portion remains;

removing said SiGe layer to form a first sidewall of said SiGe layer while said second portion remains; and

forming a second spacer on said sidewalls of said poly-silicon layer, said first blocking layer; said silicon layer, and said SiGe layer.

[c14] The method of claim 1, wherein said step of removing said second portion comprises:

removing said SiGe layer that is not part of said second portion;

applying heat to induce oxidation of said second portion at a rate faster than the oxidation of said silicon layer and said semiconductor substrate to produce an oxidation material; and

removing said oxidation material.

[c15] The method of claim 1, wherein said defining step comprises:
depositing a first blocking layer on said silicon layer;
depositing and patterning a first photoresist on said first blocking layer to form a pattern for said fin portion, said first photoresist defining said fin portion and said second portion thereunder; and
removing said first blocking layer, said silicon layer and said SiGe layer to produce said fin portion having a first sidewall and a second sidewall.

[c16] The method of claim 15, wherein said forming step comprises:
removing said first photoresist;
depositing a first insulating material on said semiconductor substrate;
depositing a gate insulating material on said first and second sidewalls;
depositing a gate layer on said first insulating material and said gate insulating material;
patterning a second photoresist defining a gate region thereunder; and
removing said poly-silicon layer and said insulating material that is not part of said gate region.

[c17] The method of claim 1, further comprising oxidizing said lower surface of said fin portion after removing said second portion.

[c18] A fin structure for a field effect transistor produced by the method of claim 1.

[c19] A fin structure for a field effect transistor comprising a silicon fin attached to a support structure, said support structure attached to a semiconductor substrate such that a void exists between said silicon fin and said semiconductor substrate.

[c20] The fin structure of claim 18, wherein said void is filled with a material selected from the group consisting of: nitride, low-k dielectric, and any combinations thereof.